operation of the processor is not affected by so doing — so it is safer to use U. The presence of two stack pointers makes the 6809 an ideal processor for use with FORTH.

- The use of the X, Y, S and U registers is not restricted to their designated modes: both S and U may be used as index registers, for example, and all four registers can be used for storing and manipulating 16-bit numbers.
- The program counter (PC) is a 16-bit register that is automatically adjusted by the processor so that it points to the next instruction. The jump (JMP) and branch (BRA) instructions alter the contents of the program counter and the 6809 allows it to be used as a type of index register. We shall look more closely at the effects of this later in the course, but by using addresses relative to the PC contents instead of specifying some absolute address stored in X or Y, the programmer can write true position-independent code. In other words, properly written programs can be loaded unaltered into any position in memory and run from there.
- The condition code register (CC) has eight bits that are used independently as flags to signal the condition of the processor. Instructions such as branch not equal (BNE) test an individual flag and cause a change in the flow of control according to the flag's condition (one or zero).

There are several instructions that are used simply for moving data into, out of and between the various registers; for the purposes of the following examples, let us suppose that we have reserved a number of memory locations by using the Assembler directives FCB and FDB. These are not instructions to the processor. When the Assembler translates the Assembly language program into machine code, it will obey them immediately and set aside the desired memory locations for program use. It will not translate the directives into machine code because they do not concern the processor. As they resemble Assembly language operation codes (such as BNE or JMP) they are sometimes called pseudo-ops;

Three's Company

Motorola's 6809 advanced 8-bit microprocessor is related to the 'old faithful' Mostech 6502 through their common ancestor, the Motorola 6800. The relation is clearly seen in their similar Assembly languages, but the 6809's register structure, with its 16-bit index registers and AB accumulator pair, more closely resembles that of the Intel-derived Zilog Z80.

The two stack registers and the direct page register are unique to the 6809, however, though the latter is plainly an advanced form of the 6502's powerful zero-page addressing facility. Technically stronger than its competitors, the 6809's late availability and the advent of 16-bit processors doomed it to a small share of the market