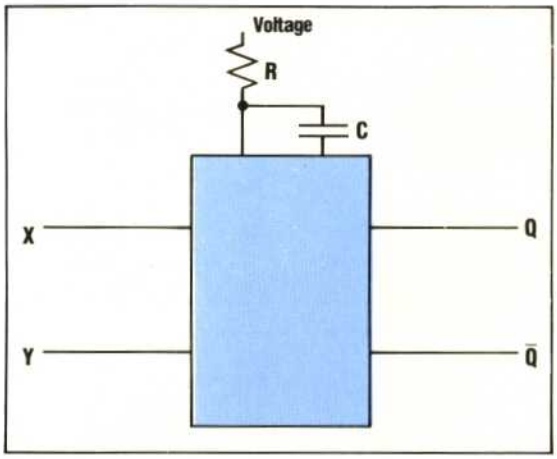
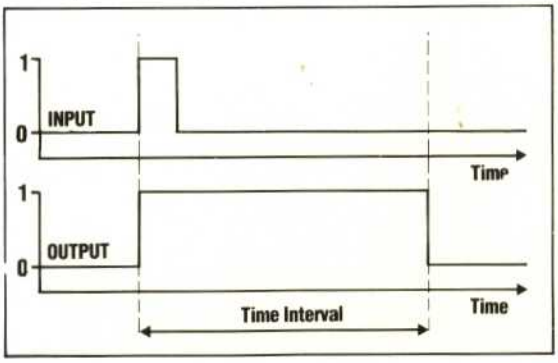
KEEPING TIME

If a computer is to control its many internal functions effectively then accurate timing is required. In this instalment we look at three types of circuit that produce timing signals — monostable circuits, D-type and J-K flip-flops. Later in the course we will investigate the use of these circuits in the design of counters and the CPU.

A *monostable circuit* provides a means of introducing fixed time intervals into logic circuit operations. When a monostable circuit receives a pulse input, the output is set to 1 (HI) for a fixed time interval before returning to its normal zero output (LO) state. The length of time for which the output goes HI is determined by the values of certain components within the circuit. This is an example of a monostable circuit:

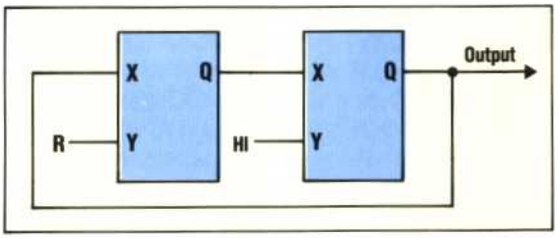


This device may be triggered by changing X from HI to LO or Y from LO to HI. By altering the values of the resistor, R, and the capacitor, C, the output time can be altered. This graph shows how the input and output are related:

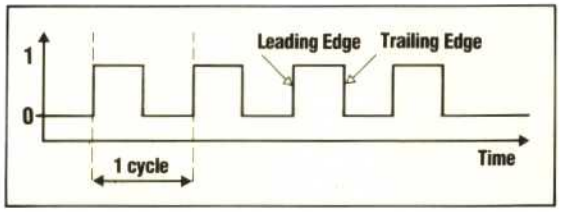


The duration of the HI output could be used to control a tape reader stepper motor or to delay the transmission of a bit for a certain length of time.

Two monostable circuits can be linked together to provide a clock pulse, which oscillates at fixed intervals between HI and LO:



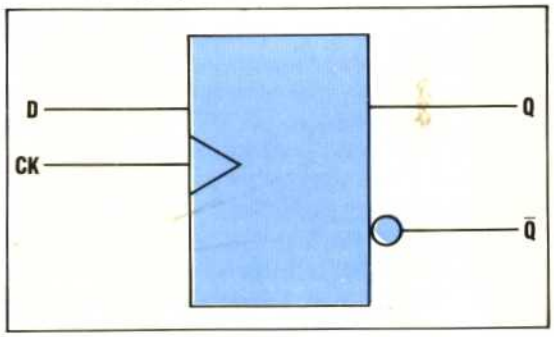
The output produced has a characteristic 'squarewave' appearance (as shown in our graphs). The time interval between the clock output going HI and the next time it goes HI is known as a cycle. Typically this is one millionth of a second. It is this continuous clock signal that is the computer's heartbeat, marshalling the many functions that are carried out in the CPU. The following diagram indicates the names given to the 'edges' of the squarewave graph, where a pulse changes from HI to LO, or vice versa:



Let us now look at two new types of flip-flop whose actions are governed by the regular pulses of the clock.

THE D-TYPE FLIP-FLOP

The D-type flip-flop has one logic input (D) and a clock input (CK):



The design of the D-type is based on the R-S flip-flop, which was discussed in the last instalment. It is the addition of the clock input, however, that causes the special method of operation known as *latching*. The output from the circuit, Q, is determined at the start of a clock cycle. If, at this time, the input at D is HI, then the output Q is set